In the Claims:

1. (Previously presented) A semiconductor device with a substrate and a semiconductor body of silicon which comprises a field effect transistor having a source region which borders on the surface of the semiconductor body and which is connected to a lower-doped, thinner source region extension and having a drain region which borders on the surface of the semiconductor body and which is connected to a lower-doped, thinner drain region extension, which regions and extensions are of a first conductivity type, and having a channel region situated between said regions and extensions, which channel region is of a second conductivity type, opposite to the first conductivity type, and having a gate electrode separated from the channel region by a dielectric region, each of the gate electrode, the source region and the drain region being provided with respective connection regions containing a metal silicide, characterized in that the source region and the source region extension, and the drain region and the drain region extension are in each case connected with each other via an intermediate region of the first conductivity type the thickness and doping concentration of which range between those of the region and the extension which are connected with one another by the intermediate region, and further wherein a sloped spacer of an electrically insulating material is situated on the semiconductor body on either side of the gate electrode and directly contacting the intermediate region and the associated extension.

2. (Previously presented) A semiconductor device as claimed in claim 1, characterized in that the connection region is recessed in the semiconductor body.

3. (Cancelled).

4. (Previously presented) A semiconductor device as claimed in claim 1, characterized in that the intermediate region is formed by means of ion implantation.

5. (Previously presented) A method of manufacturing a semiconductor device with a substrate and a semiconductor body of silicon which comprises a field effect transistor,

wherein, at the surface of the semiconductor body, a source region is formed which is connected with a lower-doped, thinner source region extension and a drain region is formed which is connected with a lower-doped, thinner drain region extension, which regions and extensions are provided with a first conductivity type, and between which a channel region of a second conductivity type, opposite to the first conductivity type, is formed which is provided with a dielectric region on which a gate electrode is formed, and wherein the source region and the drain region are provided with a connection region which comprises a metal silicide, characterized in that an intermediate region of the first conductivity type is formed in each case between the source region and the source region extension and between the drain region and the drain region extension, which intermediate region is provided with a thickness and a doping concentration which range between those of the region and the extension which are connected to one another by the intermediate region, and further characterized in that a spacer of an electrically insulating material is formed on either side of the gate electrode, and the intermediate region is formed by an ion implantation of a doping element of the first conductivity type, the ion implantation being carried out at an acute angle with the normal to the surface of the semiconductor body.

6. (Previously presented) A method as claimed in claim 5, characterized in that the metal silicide is formed by providing a metal on the semiconductor body and allowing this metal to react with silicon of the semiconductor body to form the metal silicide of the connection region.

7. (Cancelled).

8. (Previously presented) A method as claimed in claim 5, characterized in that for the angle at which the ion implantation is carried out an angle between 0 degrees and 45 degrees is chosen.

9. (Previously presented) A method as claimed in claim 5, characterized in that the ion implantation is carried out at an energy between 0.5 and 10 keV, and a flux between 5 $\times 10^{13}$ at/cm^2 and 5 $\times 10^{14}$ at/cm^2.

10. (Previously presented) A method as claimed in claim 5, characterized in that the source region and the drain region are formed by means of an additional ion implantation, and the intermediate region is formed immediately before or after the formation of the source region and the drain region, and all these regions are tempered in the same heat treatment.

11. (Previously presented) A method as claimed in claim 5, characterized in that the source region extension and the drain region extension are formed by means of an additional ion implantation step.

12. (Previously presented) A method as claimed in claim 8, wherein the angle is about 20 degrees to about 40 degrees.

13. (Previously presented) A method as claimed in claim 5, wherein the gate electrode is provided with a metal silicide layer.